REMARKS

In the Office Action, the Examiner noted that the claims 1-30 are pending in the application and that the claims 1-30 are rejected over a prior art reference. By this response, no claims have been amended. Thus, claims 1-30 remain pending in the application. Applicant respectfully traverses the rejections for the reasons indicated below.

A. Interview Summary

The undersigned attorney and Rajesh Nair thank Examiner MacArthur for the courtesy of a telephone interview on December 12, 2006. The patentability of the pending claims over cited references (US 7,024,268 ("Bennett") and US 6,517,412 ("Lee")) were discussed. The feedback controlled polishing processes of Bennett was discussed. Applicant indicated that Bennett, Lee and Cambell do not suggest a model for CMP polishing of two or more layers, as required by the claimed invention. The details of the distinction between the cited art and the claimed invention are provided in the remarks that follow.

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B. First Rejection under 35 U.S.C. §103(a)

Claims 1, 2, 4, 6, 10, 12, 13, 15, 17, 19, 23-26, 29, and 30 are rejected under 35 USC §103(a) as being obvious over Bennett et al. (US 7,024,268), hereafter "Bennett," in view of Lee et al (US 6,517,412), hereafter "Lee." Applicants respectfully traverse the rejection and respectfully submit that there is no motivation to combine the cited references to arrive at the presently claimed invention. Applicants discuss the rejection below as it applies to independent claims 1, 10, 23 and 30, and dependent claims 2, 4, 6, 12, 13, 15, 17, 19, 24-26 and 29.

The current invention is directed to methods and apparatus for polishing at least two layers of a wafer in a CMP process. Claim 1 recites "a model for CMP processing of a wafer having at least first and second layers comprising at least one control parameter, said *model comprising a first component that predicts a value for a characteristic of the first layer and a second component that predicts a value for a characteristic of the second layer*"; and "polishing at least first and second layers of a wafer" using a process recipe based on the model.